UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,407	07/29/2003	Jae-Soon Lim	5649-1132	7226

20792 7590 10/17/2005

MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,407	LIM ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is an official response to the amendment filed on 04 August 2005. The amendment canceled claim 10. Accordingly, claims 1-9 and 11-33 are currently pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5, 7-11, 14-16, 18, and 20-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Oh et al. (US 6,784100 B2).

The Oh et al. patent (Oh) discloses a method for forming a capacitor on an integrated circuit (fig. 4 and col. 4, line 10 - col. 6, line 28).

Regarding Claims 1-3, 5, 7-11, 31-33

The method for forming the capacitor comprises the following steps: forming a cylindrical lower electrode 24 of the capacitor on an integrated circuit substrate 21(fig. 4 and col. 4, lines 21-24); forming a nitride protection layer on

the cylindrical lower electrode at a temperature below a minimum temperature associated with a phase change of the cylindrical lower electrode, wherein the nitride protection layer comprises a first nitride layer 25 and a second nitride layer 26 (fig. 4; col. 4, lines 24-27; and col. 5, lines 7-30);[1] forming a dielectric layer 27 on the protection layer at a temperature less than 600°C (fig. 4 and col. 5, lines 30-42), wherein the protection layer is configured to limit oxidation of the cylindrical lower electrode during forming of the dielectric layer (col. 4, lines 24-30); and forming an upper electrode 28 of the capacitor on the dielectric layer (fig. 4 and col. 4, lines 29-32). The crystallization step, which may be performed at a temperature above 600°C, occurs after the dielectric layer is formed (see the sequence of steps described in col. 5, lines 30-58).[2] Therefore, the protection layer and the lower electrode are not exposed to a temperature above 600°C before formation of the dielectric layer.

The lower electrode 24 comprises a polycrystalline silicon layer (fig. 4 and col. 4, lines 21-24).

The nitride protection layer comprises a silicon nitride layer (col. 4, lines 24-27).

---

[1] Applicant defines the "temperature below a minimum temperature associated with a phase change of the cylindrical lower electrode" as a temperature of about 600°C or less (see specification at page 7, lines 13-20). Both layers 25 and 26 of the nitride protection layer 25, 26 are formed at a temperature ranging from 500°C-850°C. This range of temperatures includes *about 600°C or less.*

[2] The dielectric layer 27 is exposed to a temperature of 600°C to 900°C in order to crystallize the dielectric layer (col. 5, lines 54-58). Which means that not only can the crystallization step be performed at a temperature above 600°C, but it can also be performed right at 600°C.

The nitride protection layer, which comprises first silicon nitride layer 25 and second silicon nitride layer 26, is formed directly on the lower electrode. There is no intervening layer (fig. 4). The nitride layer 26 of the nitride protection layer is formed using a chemical vapor deposition process, and may be formed at a temperature of about 600°C or less (col. 5, lines 25-29 and footnote no. 1).

The dielectric layer 27 comprises a metal oxide layer (col. 4, lines 26-30).

The metal oxide layer may comprise one of a TiO_2 layer, an Al_2O_3 layer, a ZrO_2 layer, and an HfO_2 layer (col. 11, lines 7-11).

The metal oxide layer is formed using a chemical vapor deposition process, and may be formed at a temperature of about 600°C or less (col. 5, lines 30-42).

The upper electrode 28 comprises either a polycrystalline silicon layer or a composite layer of polycrystalline silicon and TiN (col. 5, lines 59-64).

The nitride protection layer comprises an electrically non-conductive layer (col. 4, lines 24-27).[3]

Regarding claims 14-16, 18, and 20-30

The method for forming the capacitor comprises the steps of: forming an insulation pattern 22 having a contact hole formed on a substrate 21 having a lower structure 23 (fig. 4 and col. 4, lines 16-22); forming a first conductive layer 24 continuously on a sidewall portion and a bottom portion of the contact

hole and on the surface of the insulation layer pattern (col. 4, line 58 - col. 5, line 3); removing the first conductive layer formed on the surface portion of the insulation layer pattern (col. 4, line 58 - col. 5, line 3); removing the insulation layer pattern to allow the first conductive layer to remain on the sidewall portion and the bottom portion of the contact hole to form a cylindrical lower electrode 24 (fig. 4 and col. 4, line 58 - col. 5, line 3); forming a reaction-preventing nitride layer 25, 26 on the first conductive layer at a temperature that does not generate a phase change of the first conductive layer (fig. 4; col. 4, lines 24-27; and col. 5, lines 7-30);[4] forming a dielectric layer 27 on the reaction-preventing nitride layer (fig. 4 and col. 4, lines 24-30), wherein the dielectric layer is formed at the temperature not generating the phase change of the first conductive layer (col. 5, lines 30-42)[5]; and forming a second conductive layer 28 on the dielectric layer (fig. 4 and col. 4, lines 29-32). Again, the crystallization step occurs after the dielectric layer is formed (refer again to the sequence of steps described in col. 5, lines 30-58). Therefore, prior to the formation of the dielectric layer, the reaction-preventing layer and the first conductive layer are not exposed to a temperature that generates a phase change of the first conductive layer.

The first conductive layer 24 comprises a polycrystalline silicon layer (fig. 4 and col. 4, lines 21-24).

---

[3] As indicated previously, the nitride protection layer 25, 26 comprises a silicon nitride layer. Silicon nitride is an electrically non-conductive layer.
[4] See Footnote No. 1.

The reaction-preventing layer 25, 26 is a silicon nitride layer (col. 4, lines 24-27).

The silicon nitride layer 26 of the reaction preventing layer is formed using a chemical vapor deposition process, and may be formed at a temperature of about 600°C or less (col. 5, lines 25-29).

The dielectric layer 27 is a metal oxide layer (col. 4, lines 26-30).

The metal oxide layer is one of a TiO_2 layer, an Al_2O_3 layer, a ZrO_2 layer, and an HfO_2 layer (col. 11, lines 7-11).

The metal oxide layer is formed using a chemical vapor deposition process, and may be formed at a temperature of about 600°C or less (col. 5, lines 30-33).

The second conductive layer 28 comprises either a polycrystalline silicon layer or a composite layer of polycrystalline silicon and TiN (col. 5, lines 59-64).

The lower structure includes a contact plug 23 connected to the lower electrode (fig. 4 and col. 4, lines 19-24).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

---

[5] The dielectric layer is formed at a temperature of 200°C to 500°C (col. 5, lines 30-42).

3. Claims 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh.

As previously discussed, both nitride layer 25 and nitride layer 26 of the protection layer/reaction-preventing layer may be formed at a temperature of about 600°C or less. In one particular embodiment, the nitride layer 25 of the protection/reaction-preventing layer 25, 26 is formed using a rapid thermal nitridation (RTN) process (col. 5, lines 7-20). In an alternate embodiment, the nitride layer 25 is formed using a plasma nitration process (col. 6, lines 11-23). Oh suggests that a plasma process may be used in place of an RTN process to form the nitride layer 25.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the nitride layer 25 using a plasma nitridation process in replace of an RTN process because rapid thermal nitridation and plasma nitridation are art-recognized equivalent surface nitriding processes that are used to form silicon nitride (col. 6, lines 40-45).

4. Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh in view of Wang (US 2003/0134486 A1).

Oh does not teach that the protection/reaction-preventing layer is formed using a microwave-type deposition process.

Wang teaches forming a silicon nitride layer 16 using one of plasma nitration, chemical vapor deposition, and remote plasma nitration, which is

a microwave-type process (fig. 2 and par. 21, lines 1-7). Wang suggests that plasma nitration, chemical vapor deposition, and remote plasma nitration are art-recognized equivalent methods for forming silicon nitride thin film layers.

As discussed above, the nitride layer 25 of the protection/reaction-preventing layer 25, 26 is formed using a plasma nitration process. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the Oh reference by forming nitride layer 25 of the protection/reaction-preventing layer using a remote plasma nitration process in place of plasma nitration, since direct plasma nitration and remote plasma nitration are art-recognized equivalent methods used for forming silicon nitride thin film layers.

5. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh in view of Dennison et al (US 5,340,765 B1).

The lower electrode 28 is formed as follows: a lower structure (not shown) is formed on the substrate 21, wherein the lower structure is a transistor (col. 4, lines 16-18); an insulation layer pattern 22 having a contact hole is formed on the lower structure (fig. 4 and col. 4, lines 16-22); a conductive plug 23 is formed in the contact hole (fig. 4 and col. 4, lines 16-22); an sacrificial layer patterned to have a cylindrical shape is formed on the insulation layer pattern and the plug (col. 4, line 58 - col. 5, line 3); a conductive layer 24 for the lower electrode is formed on the sacrificial layer (col. 4, line 58 - col. 5, line 3); and the sacrificial layer is removed to form the cylindrical lower electrode 24 (col. 4,

line 58 - col. 5, line 3). The protection layer 25, 26 is formed on the cylindrical lower electrode (fig. 4; col. 4, lines 24-27).

Oh does not teach that the sacrificial layer is an oxide layer. However, the Dennison et al. patent (Dennison) discloses a method of forming a capacitor in an integrated circuit, wherein a sacrificial layer 16 is used in the forming of a cylindrical lower electrode (see figs. 1, 2A, 4-6 and accompanying text). The sacrificial layer is an oxide layer (col. 3, lines 6-7).

Both Oh and Dennison are from the same field of endeavor, methods of forming capacitors in integrated circuits. Thus, the teaching for which Dennison is relied upon would have been recognized in the primary reference, Oh, by one having ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use an oxide layer for the sacrificial layer, as taught by Dennison, since the oxide layer has a different etching rate from that of polysilicon. By using an oxide layer for the sacrificial layer, the oxide layer is selectively etched while the polysilicon lower electrode remains substantially unetched (Dennison - fig. 6 and col. 4, lines 12-15).

Response to Arguments

6. Applicant's arguments filed on 04 August 2005 have been fully considered but they are not persuasive.

Applicant presents the following argument:

> Thus, Oh fails to disclose the methods of the present independent claims as it, in fact, teaches away from the claimed method in

> that a tantalum oxide layer is formed on the nitride layer and then exposed to high temperatures. Accordingly, the rejections of all the independent claims should be withdrawn for at least these reasons.

Each of the independent claims require: 1) that the dielectric layer is formed at a temperature of about 600°C or less, or at a temperature not generating a phase change of the first conductive layer/lower electrode; and 2) that, prior to the formation of the dielectric layer, the first conductive layer/lower electrode and the nitride protection layer/reaction-preventing layer are not exposed to a temperature above 600°C, or to a temperature that generates phase change of the first conductive layer/lower electrode. It is the examiner's position that Oh discloses both requirements. First, Applicant defines the temperature at which phase change of the first conductive layer/lower electrode does not occur as "at about 600°C or less" (see specification at page 7, lines 13-20). Oh discloses forming the dielectric layer 27, which is Ta_2O_5, at a temperature from 200°C - 500°C (col. 5, lines 30-42). Thus, Oh anticipates the limitation wherein the dielectric layer is formed at a temperature of about 600°C or less, or at a temperature not generating a phase change of the first conductive layer/lower electrode. Furthermore, Oh discloses that the crystallization step, which *may be* [emphasis added] carried out at a temperature above 600°C, is performed after the step of forming the Ta_2O_5 layer (see the sequence of steps described in col. 5, lines 30-58). Since the crystallization step takes place after the formation of the Ta_2O_5 layer, the

nitride protection layer/reaction-preventing layer 25, 26 is not exposed to a temperature above 600°C, or to a temperature that generates phase change of the first conductive layer/lower electrode prior to the formation of the Ta_2O_5 layer. Therefore, Oh anticipates the limitation wherein prior to the formation of the dielectric layer, the first conductive layer/lower electrode and the nitride protection layer/reaction-preventing layer are not exposed to a temperature above 600°C, or to a temperature that generates phase change of the first conductive layer/lower electrode. For at least these reasons, independent claims 1, 14, 24, 32, and 33 as presented in the amendment filed on 04 August 2005 do not distinguish over the prior art of record.

Applicant presents the following argument:

> For example, Claim 5 recites a chemical vapor deposition and/or atomic layer deposition process at a temperature of about 600°C or less. The Office Action, in rejecting Claim 5 recites a portion of Oh that relates to the second nitride layer 26 of Oh, which is deposited on the first nitride layer 25, not on the polysilicon layer (lower electrode) 24. Office Action, p. 5. Thus, Oh does not disclose protection layer deposited directly on the lower electrode as recited in Claim 5 as amended.

As discussed above, the nitride protection layer/reaction-preventing layer, which comprises first silicon nitride layer 25 and second silicon nitride layer 26, is formed directly on the lower electrode. There is no intervening layer. The nitride layer 26 of the nitride protection layer is formed using a chemical vapor deposition process, and may be formed at a temperature of about 600°C or less (col. 5, lines 25-29). The claim language recited in claim 5,

as presented in the amendment filed on 04 August 2005, does not preclude this interpretation.

Applicant presents the following argument:

> In rejecting Claims 4 and 17, the Office Action relies on a rapid thermal nitration embodiment described in Oh for temperatures being allegedly obvious for a different embodiment of Oh. Office Action, pp. 7-8. However, as Oh itself does not suggest the temperatures of one embodiment should be used in alternative embodiments, Applicants submit that the rejection fails to provide a particular motivation in the cited reference for modifying the teachings of the reference to arrive at the present invention as recited in Claims 4 and 1 7. Accordingly, Claims 4 and 17 are separately patentable for at least these reasons.

Please see the rejection above.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
12 October 2005

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800